DDR Clock Driver

FEATURES

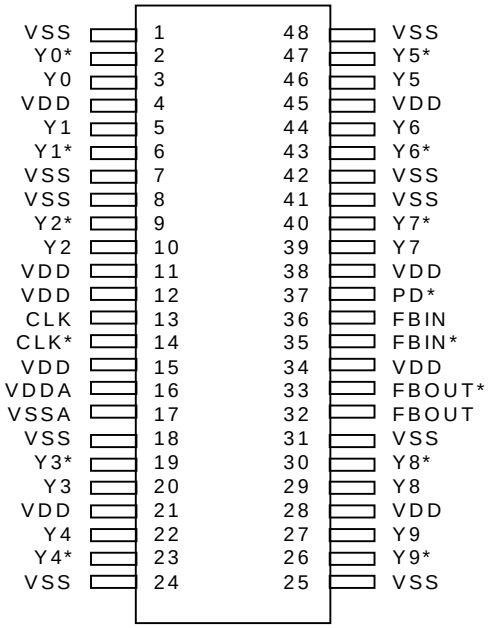
- 50% Duty Cycle Output Optimized for DDR SDRAM applications.
- 1-to-10 Differential Clock Distributions.
- Low Skew (<100pS) and Jitter (<100pS).
- 2.5V or 3.3V Vdda and 2.5V Vdd.
- SSTL_2 level clock inputs and outputs.
- Low Current Power-Down Modes.
- Available in 48-pin TSSOP Packages

DESCRIPTION

CB857 is a zero delay buffer that distributes a SSTL_2 differential clock input pair to ten SSTL_2 differential pair of low-skew, low jitter clock outputs. It uses PLL to precisely align, in both frequency and phase, the feedback clock outputs to the clock input signal. Outputs are slope controlled, signal duty cycles are adjusted to 50%, independent of the duty cycle at clock input.
A CMOS style enable/disable pin (PD*) is provided for power down mode. When PD* is low while power is applied, the PLL is turned off and the differential clock outputs are 3-stated. When the input frequency is less than approximately 20MHz, the device will enter low power shut down mode. When the input frequency increases to greater than approximately 20MHz, the PLL, and outputs will be enabled again. When VDDA is grounded, the PLL is turned off and bypassed for test purposes.

PIN ASSIGNMENT

48-Pin TSSOP Package



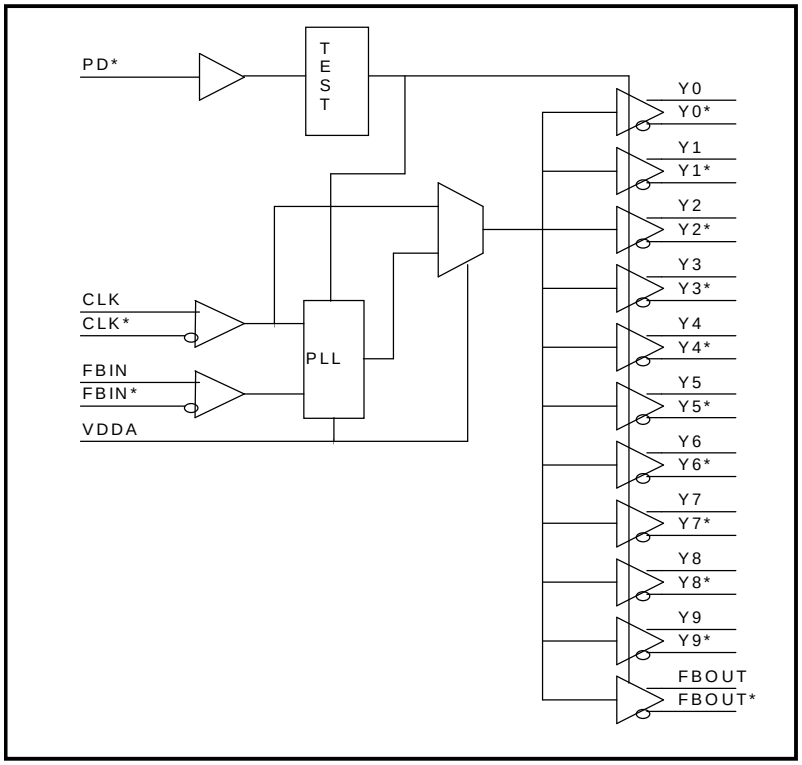


FIG. 1. FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1, 7, 8 , 18, 24, 25, 31, 41, 42, 48	VSS	Ground pins.
2, 3, 5, 6, 9, 10, 19, 20, 22, 23, 26, 27, 29, 30, 39, 40, 43, 44, 46, 47	Yn, Yn* (n=0-9)	SSTL_2 Differential Outputs. These are the low-skew copies of CLK and CLK*.
4, 11, 12, 15, 21, 28, 34	VDD	Power pins.
13, 14	CLK, CLK*,	SSTL_2 Differential Inputs. These complementary input signals provide the reference to the internal PLL that generates the clock output signals. CLK and CLK* must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK is applied, as well as following any changes to the PLL reference or feed back signals, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
16	VDDA	Analog Power. VDDA provides the power to the analog circuitry. In addition, VDDA can be used to bypass the PLL for test purposes. When VDDA is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. During disable (PD*=0), the PLL is powered down.
17	VSSA	Analog ground.
32, 33	FBOUT, FBOUT*	SSTL_2 Differential Outputs. FBOUT is used as external feedback to PLL. It switches at the same frequency as CLK. When externally wired to FBIN, it completes the loop for the PLL.

35, 36	FBIN, FBIN*	SSTL_2 Differential Inputs. These complementary input signals provide the feedback to the internal PLL. FBIN must be hard wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBI so that there is nominally zero phase error between CLK and FBI.
37	PD*	CMOS Input. Device is powered down when Low.

FUNCTIONAL DESCRIPTION

OPERATION MODES

Inputs				Outputs				PLL	Comments
Vdda	**PD***	**CLK**	**CLK***	**Y**	**Y***	**FBOUT**	**FBOUT***	**On/Off**	
X	L	X	X	Z	Z	Z	Z	Off	Power down
Normal	H	L	H	L	H	L	H	On	Operation
Normal	H	H	L	H	L	H	L	On	Operation
Normal	H	<20MHz	<20MHz	Z	Z	Z	Z	Off	Shut Off
Ground	H	L	H	L	H	L	H	Off	Bypassed
Ground	H	H	L	H	L	H	L	Off	Bypassed

Notes:
H= Logic High, L= Logic Low, Z= High impedance Off-State, X= Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MAX	NOTES
Supply Voltage	4.6V	Vdd, Vdda pins
Input Voltage	Vdd+0.5V	All Inputs
Package Dissipation	2W	TSSOP 48
Storage Temperature	-65°C to 150°C	
Junction Temperature	-55°C to 150°C	
Lead Temperature	300°C	

OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vdd	2.3	2.5	2.7	V	
Supply Current	Idd		200 100	300 200 10	mA uA uA	Vdda=Vdd, f=170MHz Vdda=Vdd, f<20MHz Vdda=Vdd, f=0MHz
Supply Analog	Vdda	2.3		2.7	V	Vdda=Vdd±0.2V
Current Analog	Idda		1	2 10 1	mA uA uA	Vdda=Vdd, f=170MHz Vdda=Vdd, f<20MHz Vdda=Vdd, f=0MHz
Operating Temp.	To	0		70	°C	

DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Voltage	Vi	-0.3		Vdd+0.3	V	CLK, FBIN, FBIN* pins

Input Differential Voltage	Vid	0.35		Vdd+0.6	V	
Input Cross Voltage	Vic	Vdd/2-.2		Vdd/2+.2	V	
Input Voltage Low	Vil			0.3xVdd	V	PD* pin
Input Voltage High	Vih	0.7xVdd			V	PD* pin
Output Voltage Low	Vol			0.1 0.6	V V	Iol=1mA Vdd=2.3V, Iol=12mA
Output Voltage High	Voh	Vdd-0.1 1.7			V V	Ioh=-1mA Vdd=2.3V, Ioh=-12mA
Output Cross Voltage	Voc	Vdd/2-.1		Vdd/2+.1		
Output Differential Voltage	Vod	0.7		Vdd+0.6	V	

AC CHARACTERISTICS

(Vss=0V; Tr=Tf≤2.5nS; Cl=50pF; Rl=1KΩ; To=0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency Operating Application	Fck	 60 95		 170 170	 MHz MHz	 Note 1. Note 2.
Input Duty Cycle	Dic	40		60	%	CLK, CLK* pins
Input Slew Rate	Rsi	1		4.0	V/nS	
Propagation Delay	Tpd	1.5	3.5	6	nS	PLL bypassed
Output Enable	Ten		3		nS	PLL bypassed
Output Disable	Tdis		3		nS	PLL bypassed
Phase Error	Tphe	-50	0	50	pS	
Output Skew	Tskw			100	pS	Identical loadings
Peak-to-Peak Jitter	Tjp	-100		100	pS	
Cycle-to-Cycle Jitter	Tjc	>-100		<100	PS	
Output Duty Cycle	Doc	49.5		50.5	%	
Output Slew Rate	Rso	1		2.0	V/nS	Rl=120Ω, Cl=14pF
Input Capacitance	Cin	2		3	PF	
Input Capacitance Delta	Cid	-0.2		0.2	PF	
Sync Time	Ts			100	US	Note 3

Notes:

1. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (used for low speed system debug.)
2. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
3. Sync time is the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal after power up. During normal operation, the sync time is also the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal when the input clock frequency falls below 20MHz, entered the power-down mode and later increased above 20MHz.

TIMING WAFEFORMS

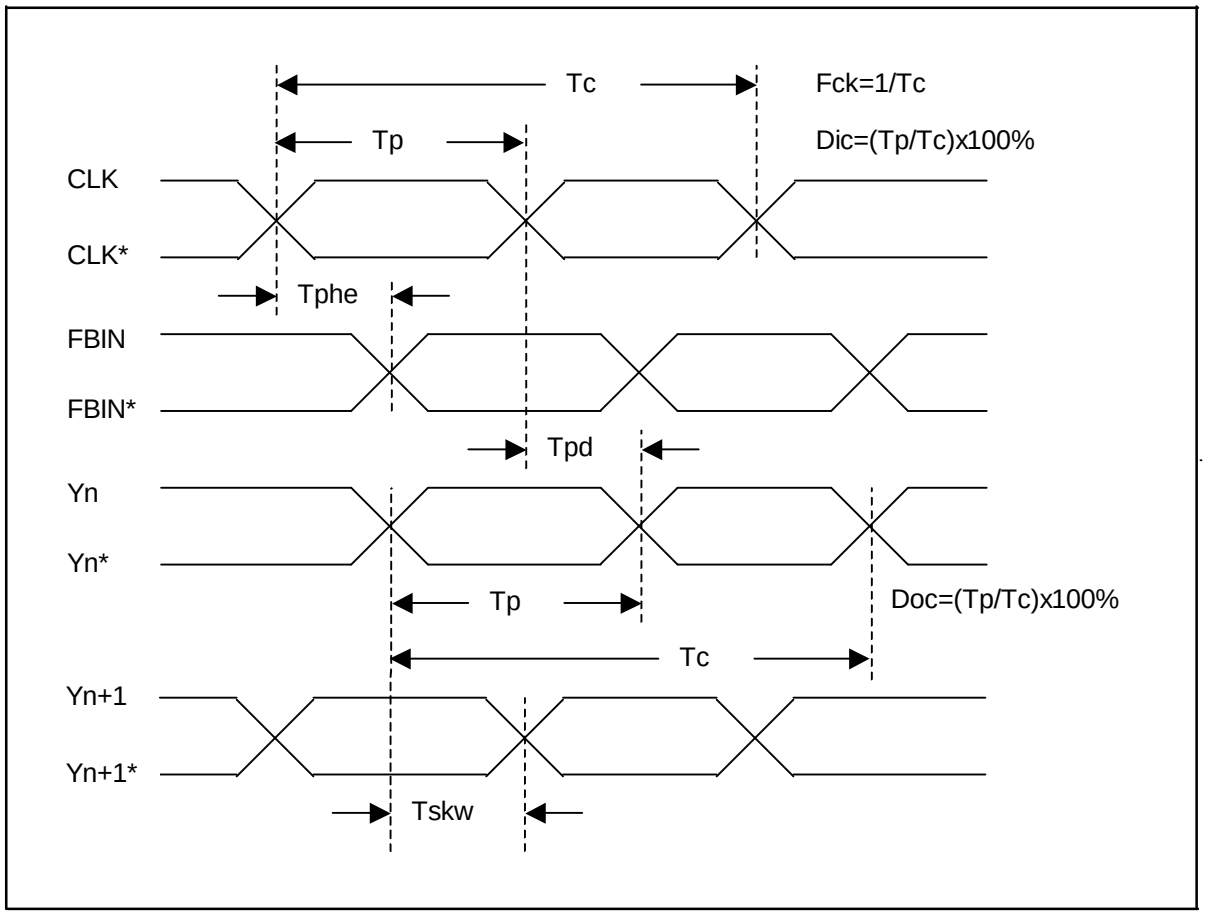


FIG. 1. Timing diagrams.

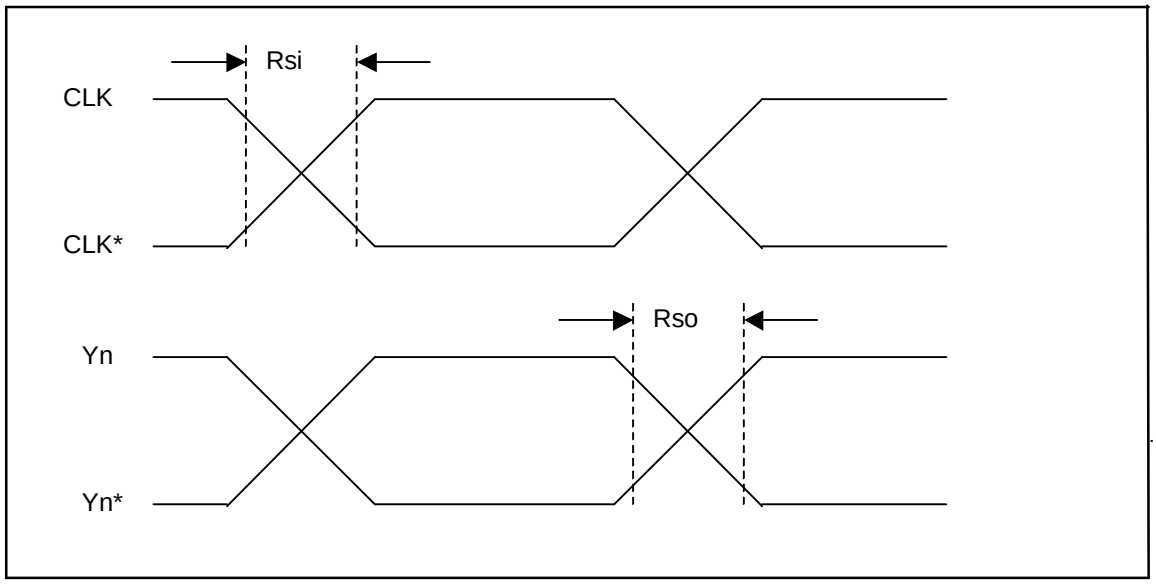
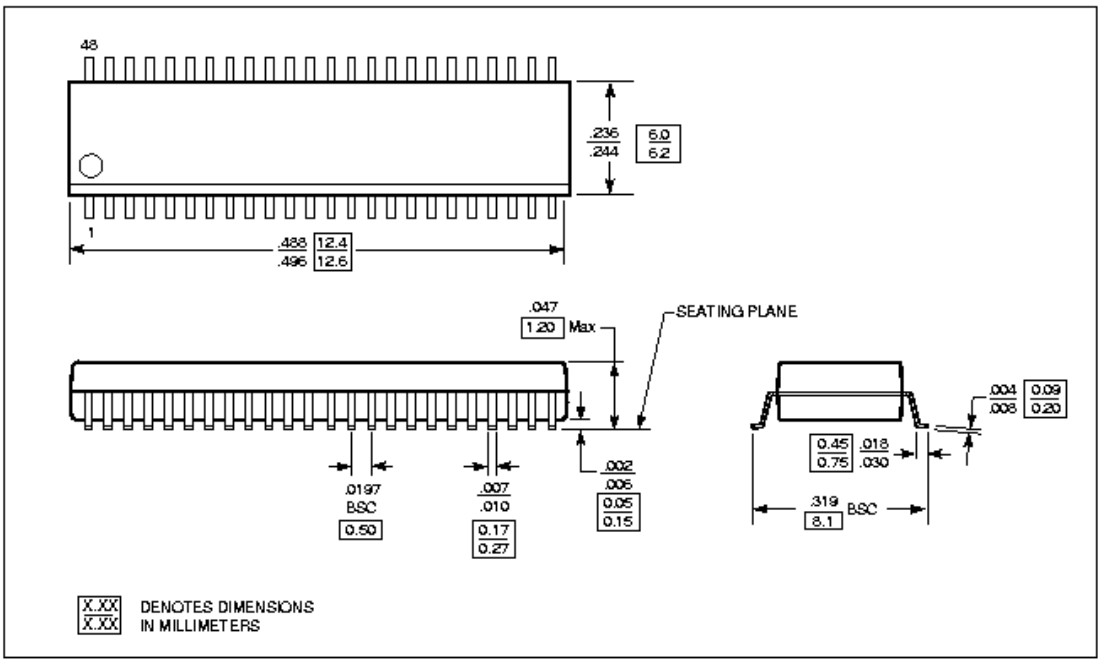


FIG. 2. Timing diagrams.

Plastic 48-Pin TSSOP Package Diagram (A)



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