

## DDR Clock Driver

### FEATURES

- 50% Duty Cycle Output Optimized for registered DDR2 DIMM applications.
- 1-to-10 Differential Clock Distributions.
- Low Skew (<40pS) and Jitter (<40pS).
- 1.8V or 2.5V Vdda and Vdd.
- LVCMOS level clock inputs and outputs.
- Low Current Power-Down Modes.
- Available in 40-pin MLF & 52-Ball VF-BGA Packages

### DESCRIPTION

CB877 is a zero delay buffer that distributes a differential input clock pair CKIN/CKIN\* to ten differential output clock pairs Y[0:9]/Y[0:9]\* and one differential feedback clock pair FBOU/FBOU\*. The output clocks are controlled by the input clock pair CKIN/CKIN\*, the feedback clock pair FBIN/FBIN\*, the LVCMOS control inputs OE, OS and the Analog Power input VDDA. When OE is Low, the outputs (except FBOU/FBOU\*) are disabled while the internal PLL continues to maintain its locked-in frequency. OS (Output Select) is a program pin that must be tied to VSS or VDD. When OS is High, OE will function as described above. When OS is Low, OE has no effect on Y7/Y7\* (they are free running in addition to FBOU/FBOU\*). When VDDA is grounded, the PLL is turned off and bypassed for test purposes. When both input clock signals CKIN/CKIN\* are logic Low, the device will enter a low power mode. An input logic detection circuit on the differential inputs, independent from the input buffer, will detect the logic Low level and perform a low power state where all outputs, the feedback and the PLL are OFF. When inputs transition from both being logic Low to being differential signals, the PLL will be turned back on, the inputs and outputs will be enabled and the PLL will obtain phase lock between the feedback clock pair FBIN/FBIN\* and the input clock pair CKIN/CKIN\* within the specified stabilization time.

The PLL in the CB877 clock driver uses the input clock CKIN/CKIN\* and the feedback clocks

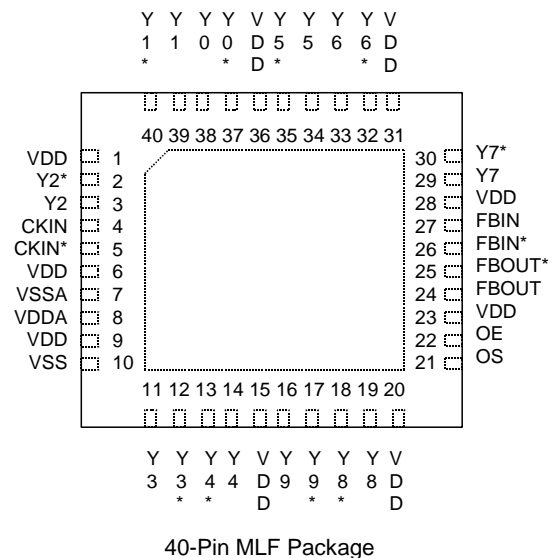
FBIN/FBIN\* to provide high-performance, low-skew, low-jitter, nearly 50% duty cycle output differential clocks Y[0:9]/Y[0:9]\*. The CB877 is also able to track Spread Spectrum Clocking (SSC) for reduced EMI.

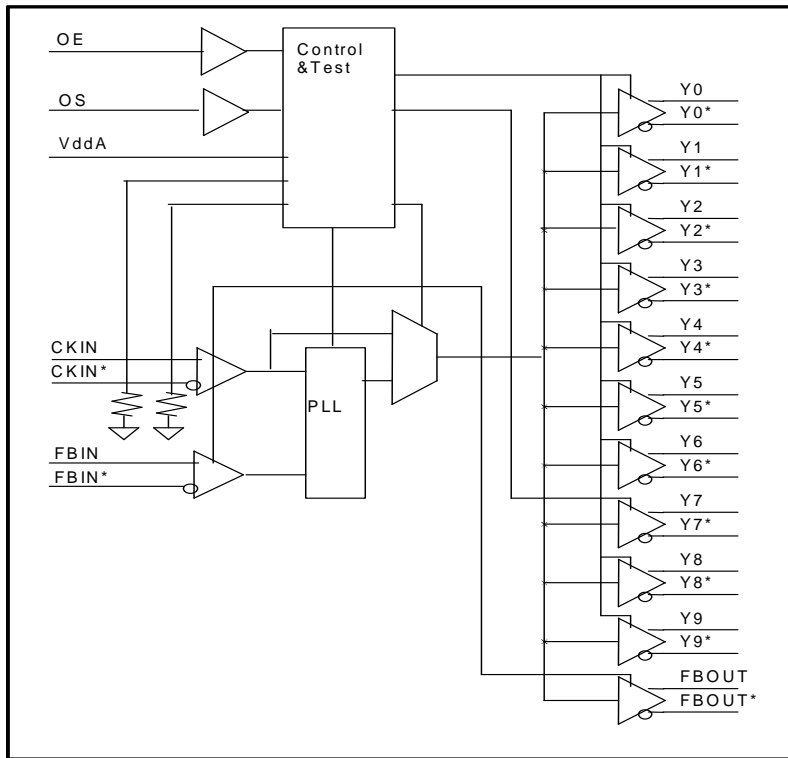
### PIN ASSIGNMENT

#### BGA Topview

Y1	Y0	Y0*	Y5*	Y5	Y6
Y1*	VSS	VSS	VSS	VSS	Y6*
Y2*	VSS	NB	NB	VSS	Y7*
Y2	VDD	VDD	VDD	OS	Y7
CKIN	VDD	NB	NB	VDD	FBIN
CKIN*	VDD	NB	NB	OE	FBIN*
VSSA	VDD	VDD	VDD	VDD	FBO*
VDDA	VSS	NB	NB	VSS	FBO
Y3	VSS	VSS	VSS	VSS	Y8
Y3*	Y4*	Y4	Y9	Y9*	Y8*

52-Ball VF-BGA (10x6 Array, 7.0x4.5mm Body Size, 0.65mm Pitch, MO-225 Variation BA package pinouts).





**FIG. 1. FUNCTIONAL BLOCK DIAGRAM**

### PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
10	VSS	Ground pins.
2, 3, 11, 12, 13, 14, 16, 17, 18, 19, 29, 30, 32, 33, 34, 35, 37, 38, 39, 40	Y <sub>n</sub> , Y <sub>n</sub> * (n=0-9)	Differential Outputs. These are the 50% shaped low-skew copies of CKIN and CKIN*.
1, 6, 9, 15, 20, 23, 28, 31, 36	VDD	Power pins.
4, 5	CKIN, CKIN*	Differential Inputs. These complementary input signals provide the reference to the internal PLL that generates the clock output signals. CKIN and CKIN* must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK is applied, as well as following any changes to the PLL reference or feed back signals, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
8	VDDA	Analog Power. VDDA provides the power to the analog circuitry. In addition, VDDA can be used to bypass the PLL for test purposes. When VDDA is strapped to VSS, PLL is bypassed and CKIN, CKIN* are buffered directly to the device outputs.
7	VSSA	Analog ground.
24, 25	FBOUT, FBOUT*	Differential Outputs. FBOUT is used as external feedback to PLL. It switches at the same phase and frequency as CKIN. When externally wired to FBIN, it completes the loop for the PLL.
27, 26	FBIN, FBIN*	Differential Inputs. These complementary input signals provide the feedback to the internal PLL. FBIN must be hard wired to

		FBOUT to complete the PLL. The integrated PLL synchronizes CKIN and FBIN so that there is nominally zero phase error between CKIN and FBIN.
22	OE	LVC MOS Input. Outputs disabled when Low.
21	OS	LVC MOS Input. Output select.

## FUNCTIONAL DESCRIPTION

### OPERATION MODES

INPUTS					OUTPUTS				PLL	
Vdda	OE	OS	CKIN	CKIN*	Y	Y*	FBOUT	FBOUT*	On/Off	Comments
Ground	H	X	L	H	L	H	L	H	Off	Bypassed
Ground	H	X	H	L	H	L	H	L	Off	Bypassed
Ground	L	H	L	H	Lz	Lz	L	H	Off	Bypassed
Ground	L	L	H	L	Lz, Y7	Lz, Y7*	H	L	Off	Bypassed
Normal	L	H	L	H	Lz	Lz	L	H	On	Operation
Normal	L	L	H	L	Lz, Y7	Lz, Y7*	H	L	On	Operation
Normal	H	X	L	H	L	H	L	H	On	Operation
Normal	H	X	H	L	H	L	H	L	On	Operation
X	X	X	L	L	Lz	Lz	Lz	Lz	Off	Shut Off
X	X	X	H	H	Reserved					

Notes:

H= Logic High, L= Logic Low, X= Don't Care, Lz= High impedance Off to Low state, Y7/Y7\*=Y7 Output pair only.

### ABSOLUTE MAXIMUM RATINGS

PARAMETER	MAX	NOTES
Supply Voltage	4.6V	Vdd, Vdda pins
Input Voltage	Vdd+0.5V	All Inputs
Package Dissipation	2W	MLF 40
Storage Temperature	-65°C to 150°C	
Junction Temperature	-55°C to 150°C	
Lead Temperature	300°C	

### OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vdd	1.7	1.8	1.9	V	
Supply Current	Idd+Idda		200 100	300 200	mA uA	Vdda=Vdd, f=270MHz, All outputs open Vdda=Vdd, f=0MHz, CKIN=CKIN*=Low
Supply Analog	Vdda		Vdd			Vdda=Vdd
Operating Temp.	To	0		70	°C	Free-air

### DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Voltage	Vi	-0.3		Vdd+0.3	V	

Preliminary specification

Input Differential Voltage	V <sub>id</sub>	0.3 0.6			V V	DC AC
Input Cross Voltage	V <sub>ix</sub>	V <sub>dd</sub> /2-.15		V <sub>dd</sub> /2+.15	V	
Input Voltage Low	V <sub>il</sub>			0.35xV <sub>dd</sub>	V	OE, OS, CKIN, CKIN*
Input Voltage High	V <sub>ih</sub>	0.65xV <sub>dd</sub>			V	OE, OS, CKIN, CKIN*
Output Voltage Low	V <sub>ol</sub>			0.1 0.6	V V	I <sub>ol</sub> =100uA V <sub>dd</sub> =1.7V, I <sub>ol</sub> =9mA
Output Voltage High	V <sub>oh</sub>	V <sub>dd</sub> -0.2 1.1			V V	I <sub>oh</sub> =-100uA V <sub>dd</sub> =1.7V, I <sub>oh</sub> =-9mA
Output Cross Voltage	V <sub>oc</sub>	V <sub>dd</sub> /2-.1		V <sub>dd</sub> /2+.1		
Output Differential Voltage	V <sub>od</sub>	0.6			V	
Output Disabled Low	I <sub>odl</sub>	100			uA	Disabled Outputs, V <sub>odl</sub> =100mV

## AC CHARACTERISTICS

(V<sub>ss</sub>=0V; Tr=Tf≤2.5nS; Cl=50pF; Rl=1KΩ; To=0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	F <sub>ck</sub>					
Operating Application		125 160		270 270	MHz MHz	Note 1. Note 2.
Input Duty Cycle	D <sub>ic</sub>	40		60	%	CKIN, CKIN* pins
Input Slew Rate	R <sub>si</sub>	1		4.0	V/nS	
Propagation Delay	T <sub>pd</sub>			8	nS	PLL bypassed
Output Enable	T <sub>en</sub>			8	nS	PLL bypassed
Output Disable	T <sub>dis</sub>			8	nS	PLL bypassed
Phase Error	T <sub>phe</sub>	-50		50	pS	V <sub>id</sub> -V <sub>od</sub>  <0.2V
Output Skew	T <sub>skw</sub>			40	pS	Identical loadings
Cycle to Cycle Jitter	T <sub>jc</sub>	-40		40	pS	
Period Jitter	T <sub>jp</sub>	-40		40	pS	
Half Period Jitter	T <sub>jh</sub>	-75		75	pS	
Output Duty Cycle	D <sub>oc</sub>	49.5		50.5	%	
Output Slew Rate	R <sub>so</sub>	1.5		3.0	V/nS	Rl=120Ω, Cl=14pF
Input Capacitance	C <sub>in</sub>	2		3	pF	
Input Capacitance Delta	C <sub>id</sub>	-0.2		0.2	pF	
Sync Time	T <sub>s</sub>			15	uS	Note 3

### Notes:

1. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (used for low speed system debug.)
2. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
3. Sync time is the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal after power up. During normal operation, the sync time is also the time required for the integrated PLL circuit to obtain phase lock of it's feedback signal to it's reference signal when the input CKIN and CKIN\* go to a logic Low state, entered the power-down mode and later return to active operation. CKIN and CKIN\* may be left floating after they have been driven Low for one complete clock cycle.

## TIMING WAVEFORMS

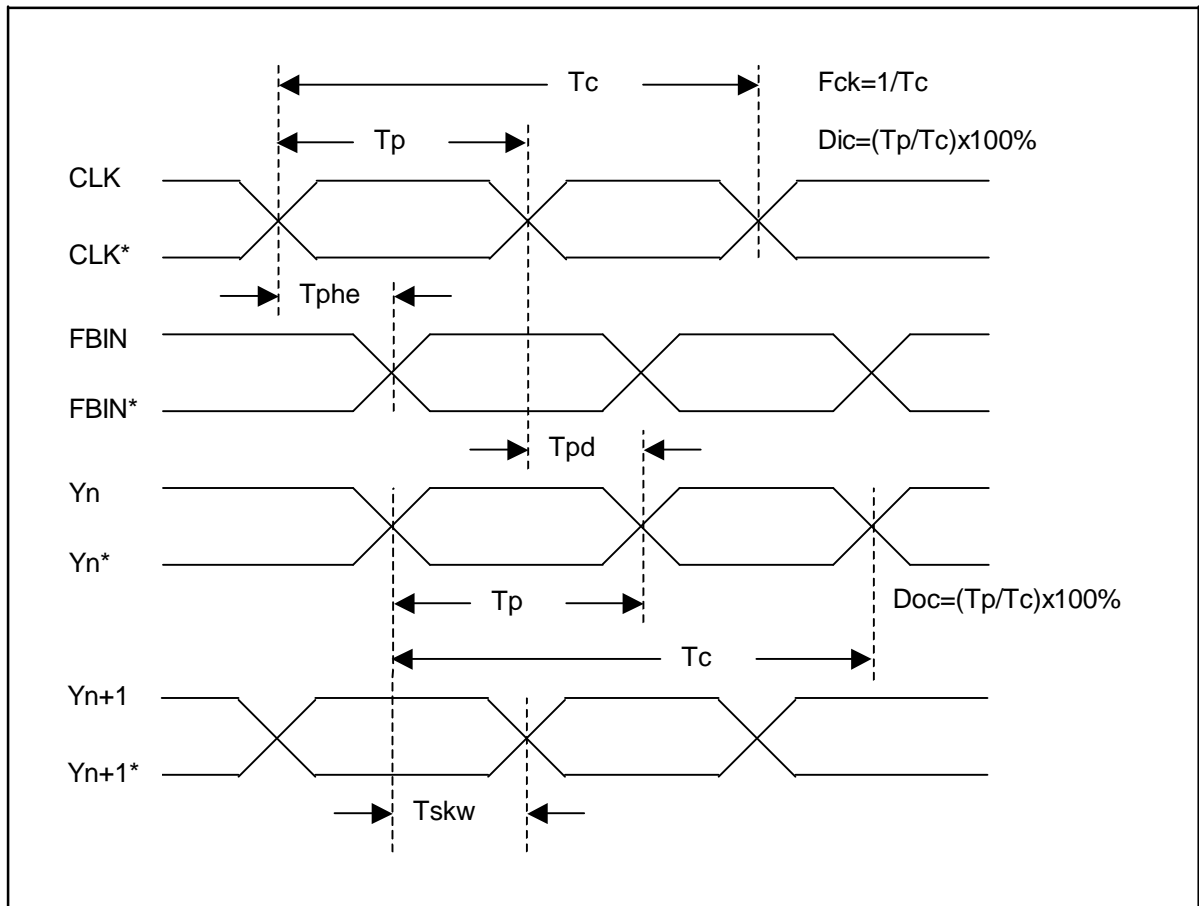


FIG. 1. Timing diagrams.

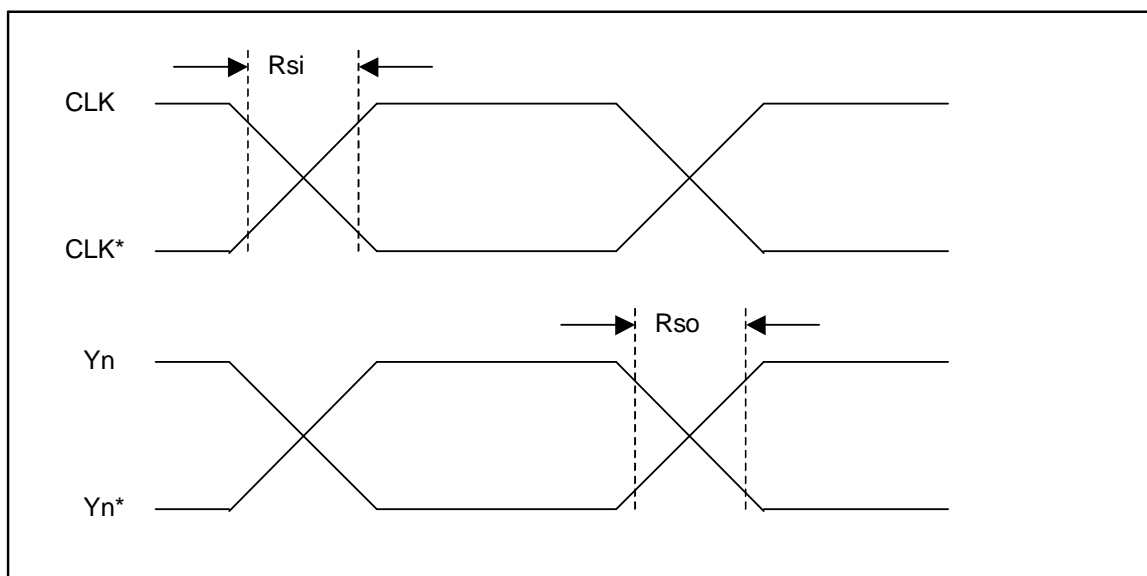


FIG. 2. Timing diagrams.

