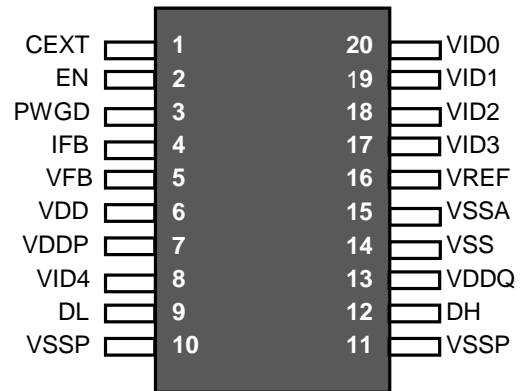


## Synchronous Mode Switching Regulator Controller

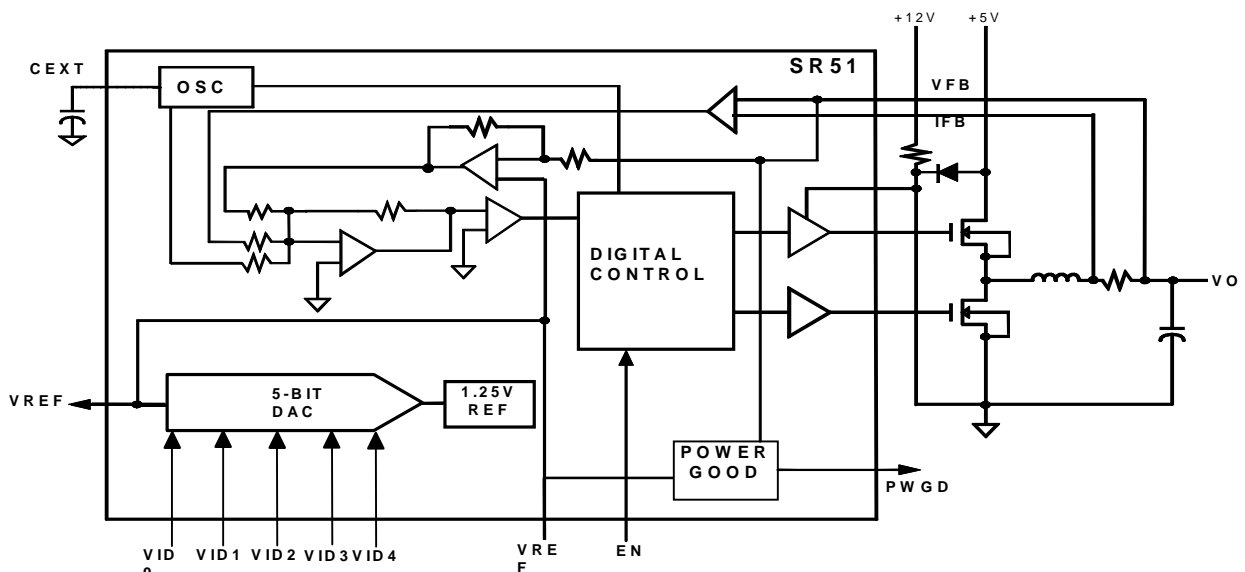
### FEATURES

- ◆ Variable output 1.3V to 3.5V from 5V input
- ◆ 85% efficiency or better
- ◆ Frequency range from 200KHz to 1MHz
- ◆ Integrated Power Good and Enable functions
- ◆ Internal Soft Start Control
- ◆ Over-voltage protection
- ◆ Short circuit protection with current limiting
- ◆ Drives N-channel MOSFETs
- ◆ 20 pin SOIC package
- ◆ Meets Intel Klamath specifications



### GENERAL DESCRIPTION

The SR51 is a synchronous mode switching regulator controller. It provides an accurate, variable output voltage for all Pentium Pro CPU applications, including Klamath. The SR51 uses a high level of integration to deliver load currents in excess of 15A from a 5V source with minimal external circuitry. Using an integrated 5-bit D/A converter, the output voltage may be selected from 1.3V to 3.5V. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. The internal oscillator may be programmed from 200KHz to 1MHz for additional flexibility in choosing external components. An on board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The SR51 also offers integrated functions including Power Good, Output Enable, Soft Start, over-voltage protection, and current limiting.



## PIN DEFINITIONS

Pin No	Pin Name	Type	Descriptions
1	CEXT	A	Connecting an external capacitor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
2	EN	I	A logic LOW on this pin will disable the output. An internal pull-up resistor allows for either open collector or TTL compatibility.
3	PWGD	OC	An open collector output that will be at logic LOW if the output voltage is not within $\pm 12\%$ of the nominal output voltage set point.
4	IFB	A	Pins 4 and 5 are used as the inputs for the current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
5	VFB	A	Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. See Application Information for details regarding correct layout.
6	VDD	P	Connect to system 5V supply and de-coupled with a 0.1 $\mu$ F ceramic capacitor.
7	VDDP	P	Power input for low side FET driver connect to system 5V supply and place a 4.7 $\mu$ F ceramic capacitor. - To ground.
8	VID4	I	A logic 1 on this open collector/TTL input will enable the VID3-VID0 inputs to set the output from 2.1V to 3.5V. A logic 0 will set the output from 1.3V to 2.05V. Pull-up resistors are internal to the controller.
9	DL	O	Low Side FET Driver connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be $< 0.5"$ .
10, 11	VSSP	P	Return pin for high currents flowing in pins 7 and 13 (VDDP and VDDQ). Connect to a low impedance ground.
12	DH	O	High Side FET Driver connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be $< 0.5"$ .
13	VDDQ	P	This is the supply for the high side FET driver. VDDQ must be connected to a voltage of at least $VDD + V_{GS, ON}$ (MOSFET).
14	VSS	P	Return path for digital logic. Connect to a low impedance system ground plane to minimize ground loops.
15	VSSA	P	Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
16	VREF	A	This pin provides access to the DAC output and should be de-coupled to ground using 0.1 $\mu$ F capacitor. No load should be connected.
17-20	VID0-VID3	I	These open collector/TTL compatible inputs will set the output voltage over the ranges specified in Table 1. Pull-up resistors are internal to the controller.

## ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings

Supply Voltages, Vddq	13V
Supply Voltage, Vdd, Vddp	7V
All Other Inputs	7V
Junction Temperature, T <sub>J</sub>	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

## Operating Conditions

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Voltage, Vdd, Vddp	4.75	5	5.25	V	VDD, VDDP pins
Input Logic HIGH	2.0			V	All digital inputs
Input Logic LOW			0.8	V	All digital inputs
Ambient Operating Temp T <sub>A</sub>	0		70	°C	
Output Driver Supply, Vddq	8.5		12	V	VDDQ pin
PWGD threshold	93		107	%V <sub>O</sub>	Logic High
	88		112	%V <sub>O</sub>	Logic Low

## DC, AC Characteristics

(V<sub>dd</sub>=5V, V<sub>OUT</sub>=2.8V, f<sub>OSC</sub>=300KHz, and T<sub>A</sub>=+25°C using circuit in Figure 1, unless otherwise noted)

The ♦ denotes specifications which apply over the full operating temperature range.

Parameter	Min	Typ.	Max.	Units		Conditions
Output Voltage	1.3	3.3	3.5	V	♦	See Table 1
Output Current		13		A		
Initial Voltage Set point		±20		mV		I <sub>LOAD</sub> =0.8A
Output Temperature Drift		+10		mV	♦	T <sub>A</sub> =0 to 60°C
Load Regulation		-25		mV	♦	I <sub>LOAD</sub> =0.8A to 13A
Line Regulation		±11		mV	♦	V <sub>IN</sub> =4.75V to 5.25V
Output Ripple		±2		mV		20MHz BW, I <sub>LOAD</sub> =13A
Output Voltage Regulation						
Steady State <sup>1</sup>	2.74	2.80	2.90	V	♦	V <sub>out</sub> =2.8V, I <sub>LOAD</sub> =0 to 13A
Transient <sup>2</sup>	2.66	2.80	2.94	V	♦	I <sub>LOAD</sub> =0.8 to 13A, 30A/μs
Output Voltage Regulation						See Note 3
Steady State <sup>1</sup>	1.74	1.80	1.90	V	♦	V <sub>OUT</sub> =1.8V
Transient <sup>2</sup>	1.70	1.80	1.90	V	♦	I <sub>LOAD</sub> =0.8 to 11A, 30A/μS
Efficiency	80	85		%	♦	I <sub>LOAD</sub> =13A, V <sub>OUT</sub> =2.8V
Output Driver Rise and Fall Time		50		nS		See Figure 3
Output Driver Non-overlap Time		50		nS		See Figure 3
Turn-on Response Time			10	mS		I <sub>LOAD</sub> =0A to 13A
Oscillator Range	200	300	1000	KHz		
Max Duty Cycle	90	95		%		PWM mode

### Notes:

1. Steady State Voltage Regulation includes Initial Voltage Set point. DC load regulation, output ripple/noise and temperature drift.
2. The output voltage measured at the regulator output will be within the voltage range specified as a result of a load transient occurring at a slew rate of 30A/μS. These specification assume a minimum of 20, 1μF ceramic capacitors are placed directly next to the CPU in order to provide adequate high-speed de-coupling. For motherboard applications, the PCB layout must exhibit no more than 0.5mΩ parasitic resistance and 1nH parasitic inductance between the regulator output and the CPU. For VRM implementation, additional bulk capacitors must be placed directly next to the CPU realizing no more than 25mΩ total ESR.
3. In order to satisfy the specified Output Voltage Regulation requirements for V<sub>OUT</sub> =1.8V, the output capacitors must exhibit no more than 7.5mΩ equivalent ESR for a motherboard application or 6.5mΩ for a VRM application.

Table 1. Output Voltage Selection Codes

VID4	VID3	VID2	VID1	VID0	V <sub>OUT</sub>
0	1	1	1	1	1.30V
0	1	1	1	0	1.35V
0	1	1	0	1	1.40V
0	1	1	0	0	1.45V
0	1	0	1	1	1.50V
0	1	0	1	0	1.55V
0	1	0	0	1	1.60V
0	1	0	0	0	1.65V
0	0	1	1	1	1.70V
0	0	1	1	0	1.75V
0	0	1	0	1	1.80V
0	0	1	0	0	1.85V
0	0	0	1	1	1.90V
0	0	0	1	0	1.95V
0	0	0	0	1	2.00V
0	0	0	0	0	2.05V
1	1	1	1	1	No CPU
1	1	1	1	0	2.1V
1	1	1	0	1	2.2V
1	1	1	0	0	2.3V
1	1	0	1	1	2.4V
1	1	0	1	0	2.5V
1	1	0	0	1	2.6V
1	1	0	0	0	2.7V
1	0	1	1	1	2.8V
1	0	1	1	0	2.9V
1	0	1	0	1	3.0V
1	0	1	0	0	3.1V
1	0	0	1	1	3.2V
1	0	0	1	0	3.3V
1	0	0	0	1	3.4V
1	0	0	0	0	3.5V



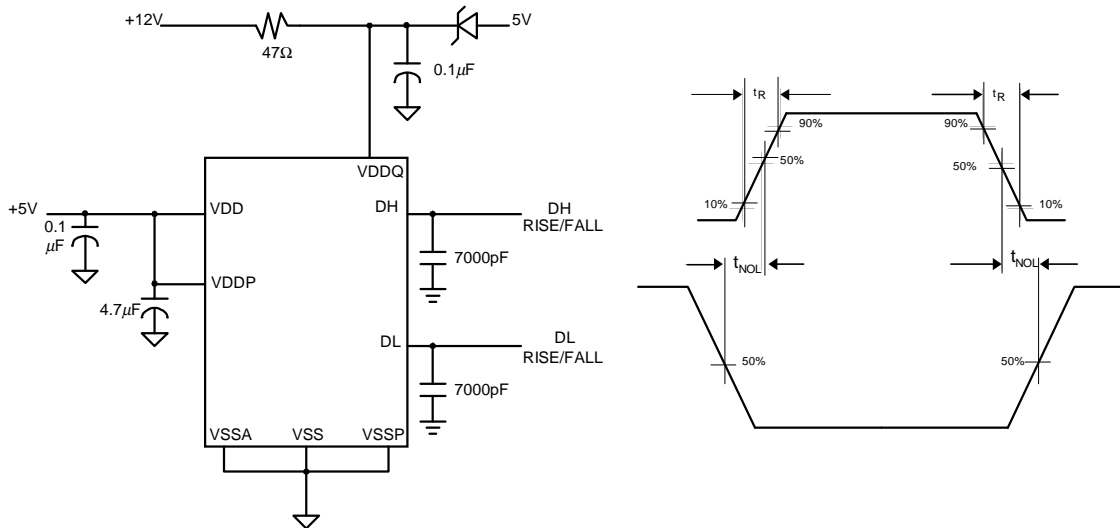


Fig. 3 Output Drive Test Circuit

Table 2. Recommended Bulk Capacitors for CPU-based Applications

Application	Output Current	C <sub>IN</sub>	C <sub>OUT</sub>	C <sub>OUT</sub> Max ESR
Intel Pentium Pro Motherboard	12.5A	3 x 1000μF, 10V United Chemi-con LXF10VB102M	4 x 1500μF, 6.3V Sanyo 6MV 1500GX	11mΩ
Intel Klamath Motherboard	13A	3 x 1000μF, 10V United Chemi-con LXF10VB102M	6 x 1500μF, 6.3V Sanyo 6MV 1500GX	7.5mΩ
Intel Klamath VRM	13A	3 x 1000μF, 10V United Chemi-con LXF10VB102M	7 x 1500μF, 6.3V Sanyo 6MV 1500GX	6.3mΩ
Motorola PowerPC 603/604 Motherboard	7A	2 x 1200μF, 10V Sanyo LXF10VB102M	3 x 1000μF, 10V Sanyo 10MV 1000CG	30mΩ

**Table 3. Bill of Materials for Intel Klamath Application**

Reference	Manufacturer Part #	Description	Conditions
C4, C5, C7-C11	Panasonic ECU-V1H104ZFX	0.1 $\mu$ F 50V capacitor	
C6	Panasonic ECSH1CY475R	4.7 $\mu$ F 16V capacitor	
Cext	Panasonic ECUV1H121JCG	100pF capacitor	
C12	Panasonic ECSH1CY105R	1 $\mu$ F 16V capacitor	
C <sub>IN</sub>	United Chemi-con LXF16VB102M10X20LL	1000 $\mu$ F 10V electrolytic capacitor 10mm x 20mm	ESR < 62m $\Omega$ See Note 1, Table 1
C <sub>OUT</sub>	Sanyo 6MV1500GX	1500 $\mu$ F 10V electrolytic capacitor 10mm x 20mm	ESR < 44m $\Omega$ See Note 1, Table 1
DS1	General Instrument 1N5817	Schottky Diode	3A, 20V
D1	1N4691	6.2V Zener Diode, Motorola	
L1	Skynet 320-8107	1.3 $\mu$ H, 14A inductor DCR ~ 6m $\Omega$	
L2	Skynet 320-6110	2.5 $\mu$ H, 11A inductor DCR ~ 6m $\Omega$	
M1, M2, M3, M4	International Rectifier IRF7413	N-Channel Logic Level Enhancement Mode MOSFET	R <sub>DS(ON)</sub> < 18m $\Omega$ V <sub>GS</sub> < 4.5V, I <sub>D</sub> = 5A
R <sub>sense</sub>	Copel CuNi Alloy resistor	6m $\Omega$ , 1W	
R5	Panasonic ERJ-6GEY050Y	47 $\Omega$ 5% resistor	
R6	Panasonic ERJ-6ENF10.0KV	10k $\Omega$ 5% resistor	

**Notes:**

1. In order to meet the voltage transient requirements for the Intel Klamath Motherboard application, the equivalent ESR of the output capacitors must not exceed 7.5m $\Omega$ . The use of the capacitors recommended in Table 1 will address this and other voltage specification without significant added cost, although it is left up to the user to specify the components used.
2. Inductor L2 is a recommended to isolate the 5V input supply from current surges caused by MOSFET switching. Lw is not required for normal operation and may be omitted if desired.

**FUNCTIONAL DESCRIPTION****The SR51 Controller**

The SR51 is a synchronous Switching regulator controller IC. When designed around the appropriate external components, the SR51 can be configured to deliver more than 15A of output current. During heavy loading conditions, the SR51 functions as a current-mode PWM step down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation), or pulse skipping mode. The controller will sense the load level and switch between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

**Main Control Loop**

Refer to the SR51 Block Diagram on page 1. The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital control block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from

the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the point at which the SR51 enters its pulse skipping mode during light loads as well as the point at which the current limit comparators disables the output drive signal to the external power MOSFETs

The digital control block takes the comparator inputs and the main clock signal from the oscillator to provide the appropriate pulses to the DH and DL output pins. These two outputs control the external power MOSFETs.

### High Current Output Drivers (DH, DL)

The SR51 contains two high current output drivers. Each driver's power and ground are separated from the chip's power and ground for additional switching noise immunity. The DH driver has a power supply VDDQ, which is supplied from an external 12V source through a series resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFET required in order to achieve a low  $R_{DS, ON}$ . Since the low side synchronous FET is referenced to ground, there is no need to boost the gate drive voltage and its VDDP power pin can be tied to VDD.

### Internal Voltage Reference (VREF)

The reference included in the SR51 is a precision bandgap voltage reference. Added to the reference input is the resulting output from an integrated 5-bit DAC. The 5-bit DAC monitors the 5 voltage identification pins VID0-VID3, as well as the range select pin (VID4). When the VID4 pin is at logic HIGH, the DAC will scale the reference voltage from 2.0V to 3.5V in 100mV increments. When VID4 is pulled LOW, the DAC will scale the reference from 1.30V to 2.05V in 50mV increments. For guaranteed stable operation under all loading conditions, 0.1 $\mu$ F of de-coupling capacitance should be connected to the VREF pin.

### Power Good (PWGD)

The SR51 Power Good function is designed in accordance with the Pentium Pro Switching regulator specification and provides a constant voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should the power supply voltage exceed  $\pm 12\%$  of its nominal set point.

### Output Enable (EN)

The SR51 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWGD output is in the low state.

### Over-Voltage Protection

The SR51 constantly monitors the output voltage for protection against over voltage conditions. If the voltage at the VFB pin exceeds 20% of the selected program voltage, an over voltage condition is assumed and the SR51 disables the output drive signal to the external MOSFETs.

### Short Circuit Protection

A current sense methodology is implemented to disable the output drive signal to the MOSFETs when an over-current condition is detected. The voltage drop created by the output current flowing across a sense resistor is presented to an internal comparator. When the voltage developed across the sense resistor exceeds the comparator threshold voltage, the SR51 reduces the output drive signal to the MOSFETs.

The Switching regulator returns to normal operation after the fault has been removed, for either an over-voltage or a short circuit condition.

### Oscillator (CEXT)

The SR51 oscillator section uses a fixed current capacitor charging configuration. An external capacitor is used to preset the oscillator frequency between 200KHz and 1MHz. This scheme allows maximum flexibility in setting the switching frequency and in choosing external components.

In general, a lower operating frequency decreases the peak ripple current flowing in the output inductor, thus allowing the use of a smaller inductor value. Unfortunately, operation at lower frequencies increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to slower loop response of the controller.

In addition, the efficiency losses due to switching of the MOSFETs increase as the operating frequency is increased. Thus, efficiency is optimized at lower frequencies. An operating frequency of 300KHz was chosen to optimize efficiency while maintaining excellent regulation and transient performance under all operation conditions.

## APPLICATION INFORMATION

### MOSFET Selection

This application requires N-channel *Logic Level* Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance,  $R_{DS, ON} < 20m\Omega$  (Lower is better)
- Low gate drive voltage,  $V_{GS} \leq 4.5V$
- Drain-Source voltage rating  $> 15V$

The on-resistance ( $R_{DS, ON}$ ) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the SR51.

### MOSFET Gate Bias

The external MOSFETs can be biased by one of two methods—Charge Pump and 12V Gate Bias. The charge pump method has the advantage of requiring only a single input voltage, but the 12V method will realize increased efficiency by providing an increased average  $V_{GS}$  to the FETs.

#### Method 1. Charge Pump (Bootstrap)

Figure 4 employs a charge pump to provide gate bias. Capacitor CP is the charge pump deployed to boost the voltage of the SR51 output driver. When the MOSFET switches off, the source of the MOSFET is at -0.6V. VDDQ is charged through the Schottky diode to 4.5V. Thus, the capacitor CP is charged to 5V. When the MOSFET turns on, the source of the MOSFET voltage is equal to 5V. The capacitor

voltage follows, and hence provides a voltage at VDDQ equal to 10V. The Schottky diode is required to provide the charge path when the MOSFET is off, and reverse bias when VDDQ goes to 10V. The charge pump capacitor(CP) needs to be a high Q, high frequency capacitor. A 1µF ceramic capacitor is recommended here.

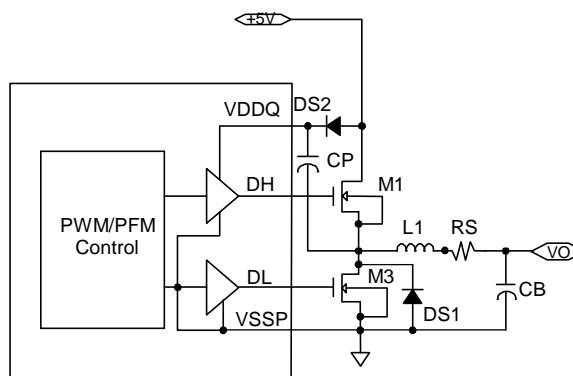


Figure 4. Charge Pump Configuration

### Method 2. 12V Gate Bias

Figure 5 illustrates how a 12V source can be used to bias VDDQ. A 47Ω resistor is used to limit the transient current into the VDDQ pin and a 1µF capacitor is used to filter the VDDQ supply. This method provides a higher gate bias voltage ( $V_{GS}$ ) to the MOSFETs, and therefore reduces the effective  $R_{DS, ON}$  and the resulting the power loss within the MOSFET. In designs where efficiency is a primary concern, the 12V gate bias method is recommended. A 6.2V Zener diode, D1, is used to clamp the voltage at VDDQ to a maximum of 12V and ensure that the absolute maximum voltage of the IC will not be exceeded.

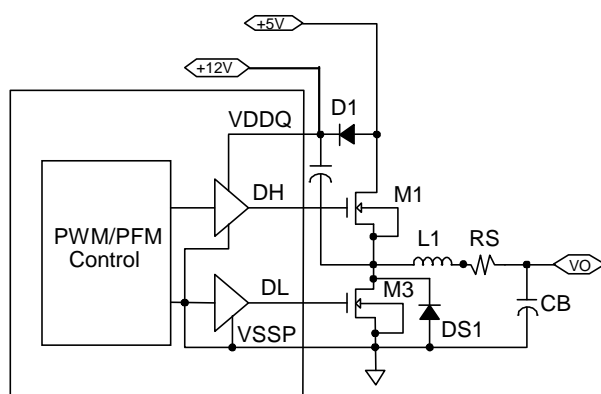


Figure 5. 12 V Gate Bias Configuration

### Inductor Selection

The inductor is one of the most critical components selected in the Switching regulator application. The critical parameters are inductance (L), maximum DC current ( $I_o$ ), and the coil resistance ( $R_l$ ). The inductor core material is a crucial factor in determining the amount of current the inductor is able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500MHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI, and low hysteresis losses,

but tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance degrades the efficiency of the regulator by the relationship:

$$P_{loss} = I_o^2 \times R_l$$

The value of the inductor is a function of the oscillator duty cycle ( $T_{ON}$ ) and the maximum inductor current ( $I_{PK}$ ).  $I_{PK}$  can be calculated from the relationship:

$$I_{pk} = I_{min} + ((V_{in} - V_{sw} - V_d)/L)T_{on}$$

Where  $T_{ON}$  is the maximum duty cycle and  $V_D$  is the forward voltage of diode DS1.

Then inductor value can be calculated using the relationship:

$$L = ((V_{in} - V_{sw} - V_o) / (I_{pk} - I_{min})) T_{on}$$

Where  $V_{sw}$  ( $R_{DS, on} \times I_o$ ) is the drain-to-source voltage of M1 when it is switched on.

### SR51 Short Circuit Current Characteristics

The SR51 short circuit current characteristic includes a hysteresis function that prevents the Switching regulator from oscillating in the event of a short circuit. Figure 6 shows the typical characteristics of the Switching regulator circuit with a 6mΩ sense resistor. The regulator exhibits a normal load regulation characteristic until the voltage across the resistor exceeds the internal short circuit threshold of 120mV. At this point, the internal comparator trips and signals the controller to turn off the gate drive to the power MOSFETs. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. The output voltage does not return to its normal value until the output current is reduced to a value within the safe operating range for the Switching regulator.

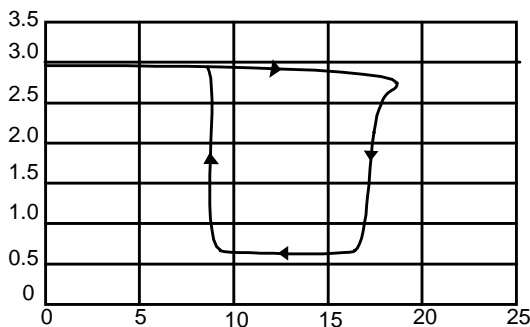


Figure 6. SR51 Short Circuit Characteristic

### Schottky Diode Selection

The application circuits of Figures 1 and 2 show a Schottky diode, DS1, which is used as a catch diode to assure there is no shorted path to ground when the upper MOSFET is turning off and the lower MOSFET is turning on. Since this time duration is very short, a 1A Schottky diode will suffice for this application.

### Output Filter Capacitors

Output ripple performance and transient response are functions of the filter capacitors. Since the 5V supply of a PC motherboard may be located several inches away from the Switching regulator, the input capacitance can play an important role in the load transient response of the SR51. The higher the input capacitance, the more charge storage is available for improving the current transfer through the FETs. Low Equivalent Series Resistance (ESR) capacitors are best suited for this type of application. Incorrect selection can hinder the regulator's overall performance. The input capacitors should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = DF / 2\pi f C$$

Where DF is the dissipation factor of the capacitor, f is the operating frequency, and C is the capacitance in farads.

With this in mind, correct calculation of the output capacitance is crucial to the performance of the Switching regulator. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu\text{F})=(I_o \times \Delta T)/(\Delta V - I_o \times \text{ESR})$$

Where  $\Delta V$  is the maximum voltage deviation due to load transients,  $\Delta T$  is the reaction time of the power source (Loop response time of the SR51 is approximately  $2\mu\text{s}$ ), and  $I_o$  is the load current step.

For  $I_o = 12.2\text{A}$  (0.8 - 13A load step) and  $\Delta V = 100\text{mV}$ , the bulk capacitance required can be approximated as follows:

$$C(\mu\text{F})=(I_o \times \Delta T)/(\Delta V - I_o \times \text{ESR})=(22.2\text{A} \times 2\mu\text{s})/(100\text{mV} - 12.2\text{A} \times 7.5\text{m}\Omega)=2870\mu\text{F}$$

Because the control loop response of the controller is not instantaneous, the initial load transient must be supplied entirely by the output capacitors. The initial voltage deviation will be determined by the total ESR of the capacitors used and the parasitic resistance of the output traces.

### Input Filter

The Switching regulator design should include an input inductor between the system +5V supply and the regulator input as described below. This inductor serves to isolate the +5V supply from the noise in the switching portion of the Switching regulator, and to limit the inrush current into the input capacitors during power up. A value of  $2.5\mu\text{H}$  is recommended.

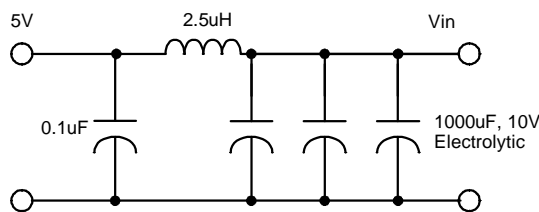


Figure 13. Input Filter

### PCB Layout Guidelines

- ◆ Placement of the MOSFETs relative to the SR51 is critical. Place the MOSFETs such that the trace length of the DH and DL pins of the SR51 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- ◆ In general, all of the noisy switching lines should be kept away from the quiet analog section of the SR51. That is traces that connect to pins 9, 12, and 13 (DL, DH and VDDQ) should be kept far away from the traces that connect to pins 1 through 5, and pin 16.
- ◆ Place the  $0.1\mu\text{F}$  de-coupling capacitors as close to the SR51 pins as possible. Extra lead length on these negates their ability to suppress noise.
- ◆ Each VDD and VSS pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- ◆ Surround the CEXT timing capacitor with a ground trace. Be sure to place a ground or power plane underneath the capacitor for the further noise isolation to provide additional shielding to the oscillator (pin 1) from the noise on the PCB. In addition, place this capacitor as close to pin 1 as possible.
- ◆ Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in #1 above. Place the input bulk capacitors as close to the drains of MOSFETs as possible. In addition, placement of a  $0.1\mu\text{F}$  de-coupling cap right on the drain of each MOSFET helps to suppress some of the high frequency switching noise on the input of the Switching regulator.
- ◆ Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the Switching regulator's performance under severe load transient conditions, causing higher voltage deviation.

- ◆ The traces that run from the SR51 IFB (pin 4) and VFB (pin 5) pins should be run together next to each other and Kelvin connected to the sense resistor. Running these lines together rejects some of the common mode noise that is presented to the SR51 feedback input. Try, as much as possible, to run the noisy switching signals (DH, DL & VDDQ) on one layer, but use the inner layers for power and ground only. If the top layer is being used to route all of the noisy switching signals, use the bottom layer to route the analog sensing signals VFB and IFB.

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