CIT STL16857

Preliminary Information

DDR Registered Driver

FEATURES

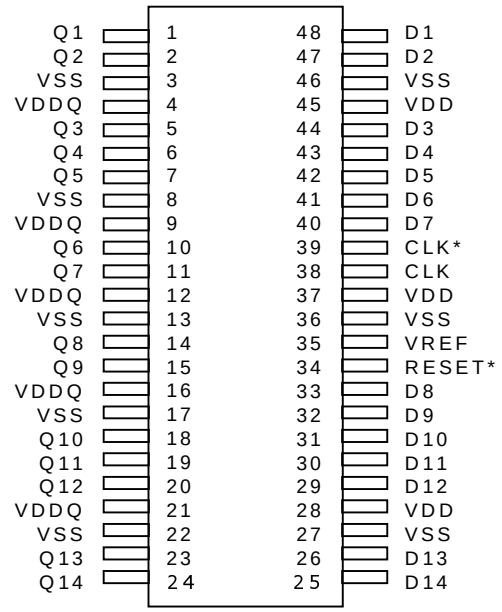
- Stub-series Terminated Logic for 2.5V Vddq.
- Optimized for DDR SDRAM Applications.
- Supports SSTL_2 Signal Inputs and Outputs.
- Flow-through Architecture Optimizes PCB Layout.
- Meets SSTL_2 Class I and Class II Specifications.
- Latch-up Protections Exceeds 500mA Per JECEC Std 17.
- ESD Protection Exceeds 2000V Per Machine Model.
- Full DDR Solution Provided When Used With CB857 and BS3857.

DESCRIPTION

The STL16857 is a 14-bit SSTL_2 registered driver with differential clock inputs. Both Vdd and Vddq support 2.5V and 3.3V operation however. Vddq must not exceed Vdd. Inputs are SSTL_2 type with Vref normally at Vddq/2. The outputs support class I which can be used for standard stub-series applications or capacitive loads. Master reset (RESET*) asynchronously resets all registers to zero.

The STL16857 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JECED, such as DDR (Double Data Rate) SDRAM or SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 100MHz will have a burst rate of 200MHz. The modules require between 23 and 27 registered control and address lines, so two 14-bit wide devices will be used on each module.

48-Pin TSSOP Package



The STL16857 is intended to be used for SSTL_2 input and output signals.

The device data inputs consist of differential receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

The clock input is fully differential to be compatible with DRAM device that are installed on the DIMM. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CLK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device must support an asynchronous input pin (reset, which when held to the LOW sate will assume that all registers are reset to the LOW state and all outputs drive a LOW signal as well.

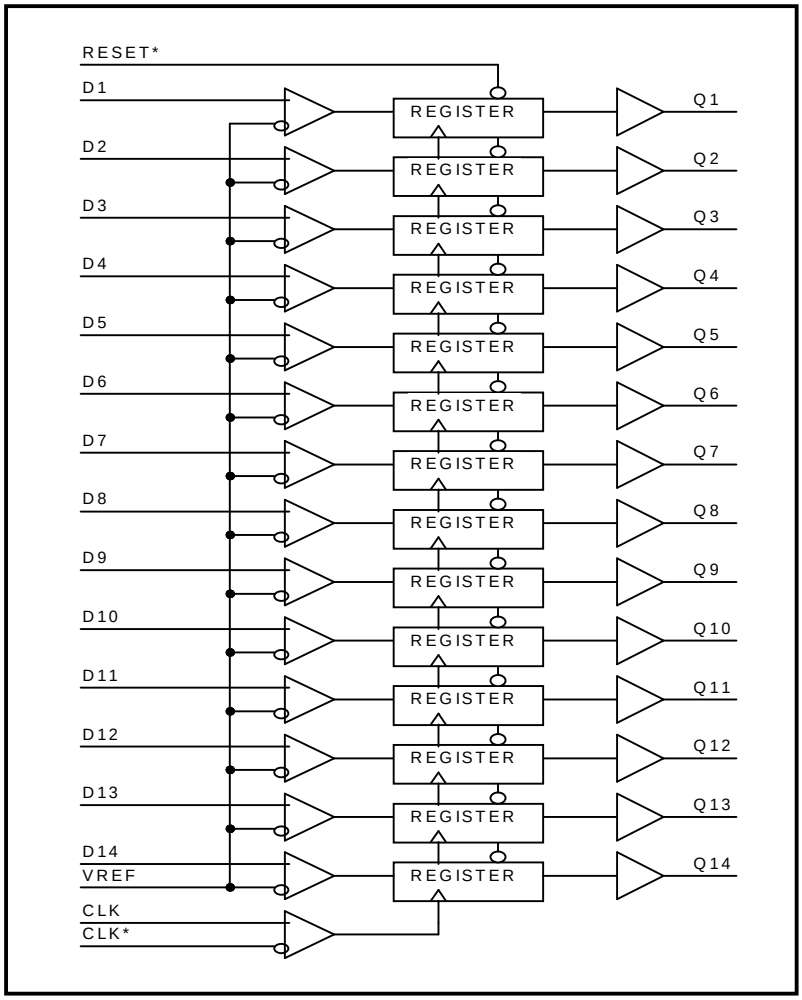


FIG. 1. FUNCTIONAL BLOCK DIAGRAM

PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
34	RESET*	LVCMOS asynchronous master reset (Active LOW)
48, 47, 44, 43, 42, 41, 40, 33, 32, 31, 30, 29, 26, 25	D1-D14	SSTL_2 data inputs
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q1-Q14	SSTL_2 data outputs
35	VREF	SSTL_2 input reference level
3, 8, 13, 17, 22, 27, 36, 46	VSS	Ground
28, 37, 45	VDD	Positive supply voltage
4, 9, 12, 16, 21	VDDQ	Output supply voltage
38	CLK	Differential clock input positive
39	CLK*	Differential clock input negative

FUNCTION TABLE

Inputs				Output
RESET*	**CLK**	**CLK***	**D**	**Q**
L	X	X	X	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0

Notes:
H = Logic High
L = Logic Low
↑ = Low-to-High transition
↓ = High-to-Low transition
X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	Vdd	Vddq	3.3	3.6	V	
Output Supply	Vddq	2.3	2.5	2.7	V	Vddq ≤ Vdd
Reference Voltage	Vref	1.15	1.25	1.35		Vref = Vddq/2
Termination Voltage	Vtt	Vref-40mV	Vref	Vref+40mV	V	
Operating Temperature	To	0		70	°C	

DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Quiescent Current	Idd			25	mA	CLK and CLK* are High
Input Voltage Low	Vil	-0.5		Vref-0.18	V	All inputs
Input Voltage High	Vih	Vref+0.18		Vddq+0.5	V	All inputs
Output Voltage Low	Vol	0 	2m 0.14 0.30	0.2 0.35 0.35	V V V	Vdd=2.3V; Iol=-100uA Vdd=2.3V; Iol=-8mA Vdd=2.3V; Iol=-16mA
Output Voltage High	Voh	 Vdd-0.2 1.95 1.95	 2.3 2.2 2.1		 V V V	Vdd=2.3V to 2.7V; Ioh=-100uA Vdd=2.3V; Ioh=-8mA Vdd=2.3V; Ioh=-16mA
Output Current High	Ioh			-20	mA	
Output Current Low	Iol			20	mA	
Common Mode	Vcmr	0.97		1.53	V	CLK, CLK*
Peak-Peak Input	Vpp	360			mV	
Input Current	Iin			5	uA	All inputs

AC CHARACTERISTICS

(Cl=10pF; 0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Voltage Low	Vih	Vref+0.35			V	All inputs
Input Voltage High	Vil			Vref-0.35		All inputs
Clock Frequency	Fck			200	MHz	CLK, CLK*
Pulse Width	Tpw	1			nS	CLK, CLK*
Setup Time	Tsu	0.8			nS	to CLK/CLK*
Hold Time	Th	0.5			nS	to CLK/CLK*
Propagation Delay	Tp	1 2		3 5	nS nS	CLK/CLK* to Q RESET* to Q

Preliminary Information

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